Errata for "Hardware implementation aspects of polar decoders and ultra high-speed LDPC decoders"

Alexios Balatsoukas-Stimming

March 27, 2017

This document is meant to provide a list of mistakes and omissions in the version of my PhD thesis that is publicly available on the website of the EPFL library under `https://infoscience.epfl.ch/record/222437/files/EPFL_TH7297.pdf`.

Chapter 2

1. In Table 2.11:
   - For Yuan et al. [63] information throughput is given, while it should be the coded throughput. Since the code is a rate-1/2 code, the correct coded throughput should be 1000 Mb/s.
   - For Che et al. [65] information throughput is given, while it should be the coded throughput. Since the code is a rate-1/2 code, the correct coded throughput should be 4002 Mb/s.
   - For Giard et al. [67] information throughput is given, while it should be the coded throughput. Since the code is a rate-1/2 code, the correct coded throughput should be 3720 Mb/s.
2. In figure 2.15, the unit on the vertical axis should be "pJ/bit" instead of "nJ/bit."
3. In Table 2.13:
   - For Yuan et al. [73] information throughput is given, while it should be the coded throughput. Since the code is a rate-1/2 code, the correct maximum coded throughput should be 9000 Mb/s while the correct sustained coded throughput should be 5176 Mb/s.
   - For Abbas et al. [74] it should be clarified that the results that are presented in the table are not included in [74] itself, but in the survey paper of [R1].
   - "Lin et al. [75]" should be "Sun et al. [75]".

References

[R1] P. Giard, G. Sarkis, A. Balatsoukas-Stimming, Y. Fan, C.-Y. Tsui, A. Burg, C. Thibeault, and W. J. Gross, "Hardware decoders for polar codes: An overview," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2016.