Alexios Balatsoukas-Stimming

Contact Details

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Education

- **PhD** in Computer and Communication Sciences — Oct 2016
  École Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland
  Thesis: Hardware implementation aspects of polar decoders and ultra high-speed LDPC decoders
  Advisor: Prof. Andreas Burg
- **MSc** in Electronic and Computer Engineering — Jun 2012
  Technical University of Crete, Chania, Greece
  Thesis: Design of LDPC codes for the two-user Gaussian multiple access channel
  Advisor: Prof. Athanasios Liavas
- **Diploma** in Electronic and Computer Engineering — Feb 2010
  Technical University of Crete, Chania, Greece
  Thesis: Analysis and design of LDPC codes for the relay channel
  Advisor: Prof. Athanasios Liavas

Positions

- **École Polytechnique Fédérale de Lausanne**, Lausanne, Switzerland — Feb 2018–present
  Postdoctoral Researcher, Telecommunications Circuits Laboratory
- **European Laboratory for Particle Physics (CERN)**, Geneva, Switzerland — Feb 2017–Jan 2018
  Marie Skłodowska-Curie Postdoctoral Fellow, Technology Department
- **École Polytechnique Fédérale de Lausanne**, Lausanne, Switzerland — Jul 2012–Jan 2017
  Graduate Researcher, Telecommunications Circuits Laboratory
- **Intel Labs**, Hillsboro, Oregon, USA — Jun 2015–Aug 2015
  Graduate Technical Intern
- **Technical University of Crete**, Chania, Greece — Mar 2010–Jun 2012
  Graduate Researcher, Telecommunications Laboratory

Honors and Awards

Marie Skłodowska-Curie fellowship, European Commission	2017
Best student paper award (2nd prize), IEEE ICECS	2015
Best student paper award finalist, IEEE ISCAS	2015
Intel employee recognition award for discipline, risk taking, and results orientation	2015
Exemplary reviewer, IEEE Wireless Communications Letters	2013 & 2014
Best student paper award (2nd prize), IEEE ICECS	2013
Special Graduate Studies Scholarship, Technical University of Crete	2010 & 2011
Two-year Scholarship for Graduate Studies, Alexander S. Onassis Foundation	2010
Scholarship of Excellence (top of class), State Scholarships Foundation of Greece	2009
Scholarship of Excellence (top of class), Technical University of Crete.	2009

Academic Activities

- **Program Committee Member:** IEEE International Conference on Communications: Full-Duplex Communications Workshop (2018), IEEE Computer Society Annual Symposium on VLSI (2018), IEEE International Workshop on Signal Processing Systems (2017), European Signal Processing Conference (2014–2018)
- **Journal Reviewer:** IEEE Transactions on Communications, IEEE Transactions on Wireless Communications, IEEE Transactions on Signal Processing, IEEE Journal on Selected Areas in Communications, IEEE Transactions on Vehicular Technology, IEEE Wireless Communications Letters, IEEE Communications

Letters, IEEE Transactions on Circuits and Systems I & II, IEEE Transactions on VLSI Systems, IEEE Journal on Emerging and Selected Topics in Circuits and Systems, IEEE Access, EURASIP Journal on Wireless Communications and Networking, Springer Journal of Signal Processing Systems

- **Conference Reviewer:** IEEE International Conference on Communications (2012, 2017), IEEE Sensor Array and Multichannel Signal Processing Workshop (2014), IEEE International Symposium on Information Theory (2015), IEEE Information Theory Workshop (2018), IEEE Wireless Communications and Networking Conference (2017–2018), IEEE International Symposium on Circuits and Systems (2015–2017), IEEE Vehicular Technology Conference (Fall 2018)
- **Web Chair:** IEEE WoWMoM ViDEv workshop (2012–2015)

Funding

- **Research Projects**
  1. Main author of Swiss National Science Foundation Project 169443 (98,424 CHF): "Gbps Decoders for Polar Codes in 5G Networks" (PI: Andreas Burg) 2016–2017
  2. Co-author of Swiss National Science Foundation Project 149447 (135,450 CHF): "Efficient ASICs for Decoding Polar Codes" (PI: Andreas Burg) 2014–2016
  3. Co-author of Swiss National Science Foundation Project 146753 (430,835 CHF): "FORTE: Full-Duplex Radios, Theory and Experiments" (PI: Andreas Burg) 2013–2017
- **Other Funding**
  1. NVIDIA Corporation GPU Grant (1x Titan Xp GPU) Feb 2018
  2. Hasler Foundation travel support grant (2,000 CHF) Sep 2017

Teaching Experience

- **Teaching Assistant**

  École Polytechnique Fédérale de Lausanne
  - *Wireless Receivers: Algorithms and Architectures* (MSc) 2012–2016
  - *Advanced Wireless Receivers: Algorithms and Architectures* (MSc) 2013–2016

  Technical University of Crete
  - *Introduction to Optimization Theory* (MSc) 2011
  - *Wireless Communications* (BSc) 2011
  - *Digital Telecommunication Systems I* (BSc) 2010, 2011
  - *Digital Telecommunication Systems II* (BSc) 2010
- **PhD Student Supervision**
  - Mr. Orion Afisiadis, PhD student at EPFL 2017–2018
    Thesis: *Beyond point-to-point full-duplex wireless communications*
  - Mr. Reza Ghanaatian, PhD student at EPFL 2017
    Thesis: *Energy-efficient wireless communications circuits through approximate computing*
- **MSc & BSc Student Supervision**
  - Mr. Yann Kurzo, MSc student at EPFL 2018
    Thesis: *FPGA implementation of a neural network self-interference canceller*
  - Ms. Tijana Stojkovic, MSc student at EPFL 2018
    Project: *Hardware implementation of an LSTM neural network*
  - Mr. Michiel Van Beirendonck, MSc exchange student (from KU Leuven) at EPFL 2018
    Project: *FPGA implementation of a Vertcoin miner*
  - Mr. Guillaume Jaume & Mr. Matthieu Cotting, MSc students at EPFL 2016
    Project: *LoRa PHY implementation and analysis*
  - Ms. Cristina Teodorescu, MSc student at EPFL 2016
    Project: *A low-power look-up table based LDPC decoder*
  - Mr. Johannes Wüthrich, BSc intern at EPFL 2015
    Project: *An FPGA-based accelerator for rapid simulation of SC polar decoders*
  - Mr. Orion Afisiadis, MSc exchange student (from University of Thessaloniki) at EPFL 2014
    Thesis: *A low-complexity improved successive cancellation decoder for polar codes*
  - Ms. Hamedeh Jafari, MSc student at EPFL 2013
    Project: *Exploiting the error-resilience of polar decoders under unreliable silicon*
- **Public Outreach**

Official tour guide at the European Laboratory for Particle Physics (CERN) 2017–2018

Languages

- Greek: Native proficiency
- German: Native proficiency
- English: Full professional proficiency
- French: Limited working proficiency

Publications

Under Review

1. P. Giard, **A. Balatsoukas-Stimming**, and A. Burg, "On the tradeoff between accuracy and complexity in blind detection of polar codes," in *International Symposium on Turbo Codes & Iterative Information Processing*, Dec. 2018
2. **A. Balatsoukas-Stimming** and A. Filos-Ratsikas, "On the computational complexity of blind detection of binary linear codes," in *IEEE Information Theory Workshop*, Nov. 2018
3. Y. Kurzo, **A. Balatsoukas-Stimming**, and A. Burg, "Design and implementation of a neural network aided self-interference cancellation scheme," in *Asilomar Conference on Signals, Systems, and Computers*, Oct. 2018

Refereed Journal Publications

1. **A. Balatsoukas-Stimming** and A. Burg, "Faulty successive cancellation decoding of polar codes for the binary erasure channel," *IEEE Transactions on Communications*, Jun. 2018
2. **A. Balatsoukas-Stimming** and A. P. Liavas, "Design of LDPC codes for the unequal power two-user Gaussian multiple access channel," *IEEE Wireless Communications Letters*, Apr. 2018
3. R. Ghanaatian, **A. Balatsoukas-Stimming** C. Müller, M. Meidlinger, G. Matz, A. Teman, and A. Burg, "A 588 Gbps LDPC decoder based on finite-alphabet message passing," *IEEE Transactions on Very Large Scale Integration Systems*, Feb. 2018
4. P. Giard, **A. Balatsoukas-Stimming**, T. Müller, A. Bonetti, C. Thibeault, W. J. Gross, P. Flatresse, and A. Burg, "PolarBear: A 28 nm FD-SOI ASIC for decoding of polar codes," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, Sep. 2017
5. P. Giard, **A. Balatsoukas-Stimming**, G. Sarkis, C. Thibeault, and W. J. Gross, "Low-complexity polar decoders for low-rate codes," *Springer Journal of Signal Processing Systems*, Mar. 2016
6. **A. Balatsoukas-Stimming**, A. C. M. Austin, P. Belanovic, and A. Burg, "Baseband and RF hardware impairments in full-duplex wireless systems: Experimental characterisation and suppression," *EURASIP Journal on Wireless Communications and Networking (Special Issue on Experimental Evaluation in Wireless Communications)*, May 2015
7. **A. Balatsoukas-Stimming**, M. Bastani Parizi, and A. Burg, "LLR-based successive cancellation list decoding of polar codes," *IEEE Transactions on Signal Processing*, Mar. 2015
8. **A. Balatsoukas-Stimming**, A. J. Raymond, W. J. Gross, and A. Burg, "Hardware architecture for list successive cancellation decoding of polar codes," *IEEE Transactions on Circuits and Systems II: Express Briefs*, Aug. 2014
9. **A. Balatsoukas-Stimming** and A. Burg, "Density evolution for min-sum decoding of LDPC codes under faulty message storage," *IEEE Communications Letters*, May 2014

Refereed Conference Publications

1. **A. Balatsoukas-Stimming**, "Non-linear digital self-interference cancellation for in-band full-duplex radios using neural networks," in *IEEE International Workshop on Signal Processing Advances in Wireless Communications (SPAWC)*, Jun. 2018
2. **A. Balatsoukas-Stimming**, T. Podzorny, and J. Uythoven, "Polar coding for the large hadron collider: Challenges in code concatenation," in *Asilomar Conference on Signals, Systems, and Computers*, Nov. 2017
3. F. Sheikh, M. Rahman, D. Yoon, **A. Balatsoukas-Stimming**, O. Andersson, D. Dasalukunte, A. Sharma, and A. Chun, "Adaptive and multi-mode baseband systems for next generation wireless communication," in *Asilomar Conference on Signals, Systems, and Computers*, Nov. 2017
4. O. Afisiadis, A. C. M. Austin, **A. Balatsoukas-Stimming**, and A. Burg, "Analysis of full-duplex wireless links with asymmetric capacity requirements," in *Asilomar Conference on Signals, Systems, and Computers*, Nov. 2017

5. P. Giard, **A. Balatsoukas-Stimming**, and A. Burg, "Blind detection of polar codes," in *IEEE International Workshop on Signal Processing Systems (SiPS)*, Oct. 2017
6. **A. Balatsoukas-Stimming**, P. Giard, and A. Burg, "Comparison of polar decoders with existing LDPC and Turbo decoders," in *IEEE Wireless Communications and Networking Conference (WCNC)*, Mar. 2017
7. P. Giard, **A. Balatsoukas-Stimming**, T. C. Müller, A. Burg, C. Thibeault, and W. Gross, "A multi-Gbps unrolled hardware list decoder," in *Asilomar Conference on Signals, Systems, and Computers*, Nov. 2016
8. A. C. M. Austin, **A. Balatsoukas-Stimming**, and A. Burg, "Digital predistortion of power amplifier non-linearities for full-duplex transceivers," in *IEEE International workshop on Signal Processing Advances in Wireless Communications (SPAWC)*, Jul. 2016
9. F. Sheikh, **A. Balatsoukas-Stimming**, and C.-H. Chen, "High-throughput lattice reduction for large-scale MIMO systems based on Seysen's algorithm," in *IEEE International Conference on Communications (ICC)*, May 2016
10. O. Afisiadis, A. C. M. Austin, **A. Balatsoukas-Stimming**, and A. Burg, "Sliding window spectrum sensing for full-duplex cognitive radios with low access-latency," in *IEEE Vehicular Technology Conference*, May 2016
11. S. A. Hashemi, **A. Balatsoukas-Stimming**, P. Giard, C. Thibeault, and W. J. Gross, "Partitioned successive-cancellation list decoding of polar codes," in *IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP)*, Mar. 2016
12. P. Giard, G. Sarkis, **A. Balatsoukas-Stimming**, Y. Fan, C.-Y. Tsui, A. Burg, C. Thibeault, and W. J. Gross, "Hardware decoders for polar codes: An overview," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2016
13. J. Wüthrich, **A. Balatsoukas-Stimming**, and A. Burg, "An FPGA-based accelerator for rapid simulation of SC decoding of polar codes," in *IEEE International Conference on Electronics, Circuits, and Systems (ICECS)*, Dec. 2015 (**best paper award**, 2nd prize)
14. M. Meidlinger, **A. Balatsoukas-Stimming**, A. Burg, and G. Matz, "Quantized message passing for LDPC codes," in *Asilomar Conference on Signals, Systems, and Computers*, Nov. 2015
15. J. Mu, A. Vosoughi, J. Andrade, **A. Balatsoukas-Stimming**, G. Karakonstantis, A. Burg, G. Falcao, V. Silva, and J. R. Cavallaro, "The impact of faulty memory bit cells on the decoding of spatially-coupled LDPC codes," in *Asilomar Conference on Signals, Systems, and Computers*, Nov. 2015
16. **A. Balatsoukas-Stimming**, M. Meidlinger, R. Ghanaatian, G. Matz, and A. Burg, "A fully-unrolled LDPC decoder based on quantized message passing," in *IEEE International Workshop on Signal Processing Systems (SiPS)*, Oct. 2015
17. **A. Balatsoukas-Stimming**, M. Bastani Parizi, and A. Burg, "On metric sorter architectures for list successive cancellation decoding of polar codes," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2015 (**best paper award finalist**)
18. O. Afisiadis, **A. Balatsoukas-Stimming**, and A. Burg, "A low-complexity improved successive cancellation decoder for polar codes," in *Asilomar Conference on Signals, Systems, and Computers*, Nov. 2014
19. **A. Balatsoukas-Stimming** and A. Burg, "Faulty successive cancellation decoding of polar codes for the binary erasure channel," in *International Symposium on Information Theory and Applications (ISITA)*, Oct. 2014
20. **A. Balatsoukas-Stimming**, G. Karakonstantis, and A. Burg, "Enabling complexity-performance trade-offs for successive cancellation decoding of polar codes," in *IEEE International Symposium on Information Theory (ISIT)*, Jun. 2014
21. K. Alexandris, **A. Balatsoukas-Stimming**, and A. Burg, "Measurement-based characterization of residual self-interference on a full-duplex MIMO testbed," in *IEEE Sensor Array and Multichannel Signal Processing Workshop (SAM)*, Jun. 2014
22. **A. Balatsoukas-Stimming**, M. Bastani Parizi, and A. Burg, "LLR-based successive cancellation list decoding of polar codes," in *IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP)*, May 2014
23. **A. Balatsoukas-Stimming**, P. Belanovic, K. Alexandris, and A. Burg, "On self-interference suppression methods for low-complexity full-duplex MIMO," in *Asilomar Conference on Signals, Systems, and Computers*, Nov. 2013
24. **A. Balatsoukas-Stimming**, N. Preyss, A. Cevrero, A. Burg, and C. Studer, "A parallelized layered QC-LDPC decoder for IEEE 802.11ad in 40 nm CMOS," in *IEEE International New Circuits and Systems Conference (NEWCAS)*, Jun. 2013
25. **A. Balatsoukas-Stimming** and A. Dollas, "FPGA-based design and implementation of a multi-Gbps LDPC decoder," in *International Conference on Field Programmable Logic and Applications (FPL)*, Aug. 2012

Invited Talks

1. "Communications hardware in the post-happy-scaling era," Technical University of Crete, Greece, Chania (hosted by Prof. A. Deligiannakis), May 16, 2018
2. "Communications hardware meets information theory and machine learning," IMT Atlantique (ex-Telecom Bretagne), Brest, France (hosted by Prof. Vincent Gripon), Mar. 21, 2018
3. "Communications hardware meets information theory and machine learning," Mathematical and Algorithmic Sciences Lab, Huawei Technologies France, Paris (hosted by Dr. Ingmar Land), Mar. 20, 2018
4. "Full-duplex communications: Self-interference cancellation and beyond point-to-point applications," University of California, Irvine, USA (hosted by Prof. Ahmed Eltawil), Feb. 16, 2018
5. "Full-duplex communications: Self-interference cancellation and beyond point-to-point applications," Qualcomm, San Diego, USA (hosted by Dr. Gabi Sarkis), Feb. 14, 2018
6. "Communications hardware meets information theory and machine learning," Information Theory and Applications (ITA) Workshop Graduation Day, Feb. 14, 2018
7. "Polar decoding on faulty hardware," Swisscom Innovation, Bern, Switzerland (hosted by Dr. Pavle Belanovic), Sep. 20 2016
8. "Complexity and energy efficiency of LDPC decoders and an initial comparison to polar codes," *Workshop on energy-efficiency in error-correction coding*, Télécom ParisTech, Paris, France, Jun. 8 2016
9. "Faulty successive cancellation decoding of polar codes for the binary erasure channel," McGill University, Montréal, Canada (hosted by Prof. Warren J. Gross), May 26 2016
10. "From coding theory to coding practice: Hardware implementation of polar decoders and Terabit/s LDPC decoders," Information Theory and Applications (ITA) Workshop Graduation Day, Feb. 2016
11. "LDPC codes," Invited tutorial talk at Intracom Telecom, Athens, Greece, Dec. 2011

Patents

1. F. Sheikh and **A. Balatsoukas-Stimming**, "Lattice reduction-aided symbol detection," WO Patent Application WO2 017 074 405, May, 2015

Demos

1. A. C. M. Austin, O. Afisiadis, **A. Balatsoukas-Stimming**, and A. Burg, "Concurrent spectrum sensing and transmission for cognitive radio using self-interference cancellation," in *ACM International Symposium on Mobile Ad Hoc Networking and Computing (MobiHOC)*, Jun. 2015
2. P. Belanovic, **A. Balatsoukas-Stimming**, and A. Burg, "A multipurpose testbed for full-duplex wireless communications," in *IEEE International Conference on Electronics, Circuits, and Systems (ICECS)*, Dec. 2013 (**best paper award**, 2nd prize)